Discontinued (9/98 - last order; 3/99 last ship)

IBM0118160 IBM0118160M
IBM0118160B IBM0118160P

1M x 16 10/10 DRAM

Features

- 1,048,576 word by 16 bit organization
- Single 3.3V ± 0.3V or 5.0V ± 0.5V power supply
- Standard Power (SP) and Low Power (LP)
- 1024 Refresh Cycles
  - 16 ms Refresh Rate (SP version)
  - 128 ms Refresh Rate (LP version)
- High Performance:

		-50	-60	Units
t_{RAC}	$\overline{RAS}$ Access Time	50	60	ns
t_{CAC}	$\overline{CAS}$ Access Time	13	15	ns
t_{AA}	Column Address Access Time	25	30	ns
t_{RC}	Cycle Time	95	110	ns
t_{PC}	Fast Page Mode Cycle Time	35	40	ns

- Low Power Dissipation
  - Active (max) - 120 mA / 100 mA
  - Standby: TTL Inputs (max) - 2.0 mA
  - Standby: CMOS Inputs (max)
    - 1.0 mA (SP version)
    - 0.1 mA (LP version)
  - Self Refresh (LP version only)
    - 200µA (3.3 Volt)
    - 300µA (5.0 Volt)
- 2 $\overline{CAS}$
- Read-Modify-Write
- $\overline{RAS}$ Only and $\overline{CAS}$ before $\overline{RAS}$
- Hidden Refresh
- Package:
  - TSOP-II 50/44 (400mil x 825mil)
  - SOJ 42/42 (400mil)

Description

The IBM0118160 is a dynamic RAM organized 1,048,576 words by 16 bits, which has a very low “sleep mode” power consumption option. These devices are fabricated in IBM’s advanced 0.5µm CMOS silicon gate process technology. The circuit and process have been carefully designed to provide high performance, low power dissipation, and high reliability. The devices operate with a single 3.3V ± 0.3V or 5.0V ± 0.5V power supply. The 20 addresses required to access any bit of data are multiplexed (10 are strobed with $\overline{RAS}$, 10 are strobed with $\overline{CAS}$).

Pin Assignments (Top View)

50/44 TSOP

Vcc	1	50	Vss
IO0	2	49	IO15
IO1	3	48	IO14
IO2	4	47	IO13
IO3	5	46	IO12
Vcc	6	45	Vss
IO4	7	44	IO11
IO5	8	43	IO10
IO6	9	42	IO9
IO7	10	41	IO8
NC	11	40	NC
NC	15	36	NC
NC	16	35	$\overline{LCAS}$
$\overline{WE}$	17	34	$\overline{UCAS}$
$\overline{RAS}$	18	33	$\overline{OE}$
NC	19	32	A9
NC	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
Vcc	25	26	Vss

42/42 SOJ

Vcc	1	42	Vss
IO0	2	41	IO15
IO1	3	40	IO14
IO2	4	39	IO13
IO3	5	38	IO12
Vcc	6	37	Vss
IO4	7	36	IO11
IO5	8	35	IO10
IO6	9	34	IO9
IO7	10	33	IO8
NC	11	32	NC
NC	12	31	$\overline{LCAS}$
$\overline{WE}$	13	30	$\overline{UCAS}$
$\overline{RAS}$	14	29	$\overline{OE}$
NC	15	28	A9
NC	16	27	A8
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
Vcc	21	22	Vss

Pin Description

$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$ / $\overline{UCAS}$	L/U Column Address Strobe
$\overline{WE}$	Read/Write Input
A0 - A9	Address Inputs
$\overline{OE}$	Output Enable
I/O0 - I/O15	Data Input/Output
V_{CC}	Power (+3.3V or +5.0V)
V_{SS}	Ground

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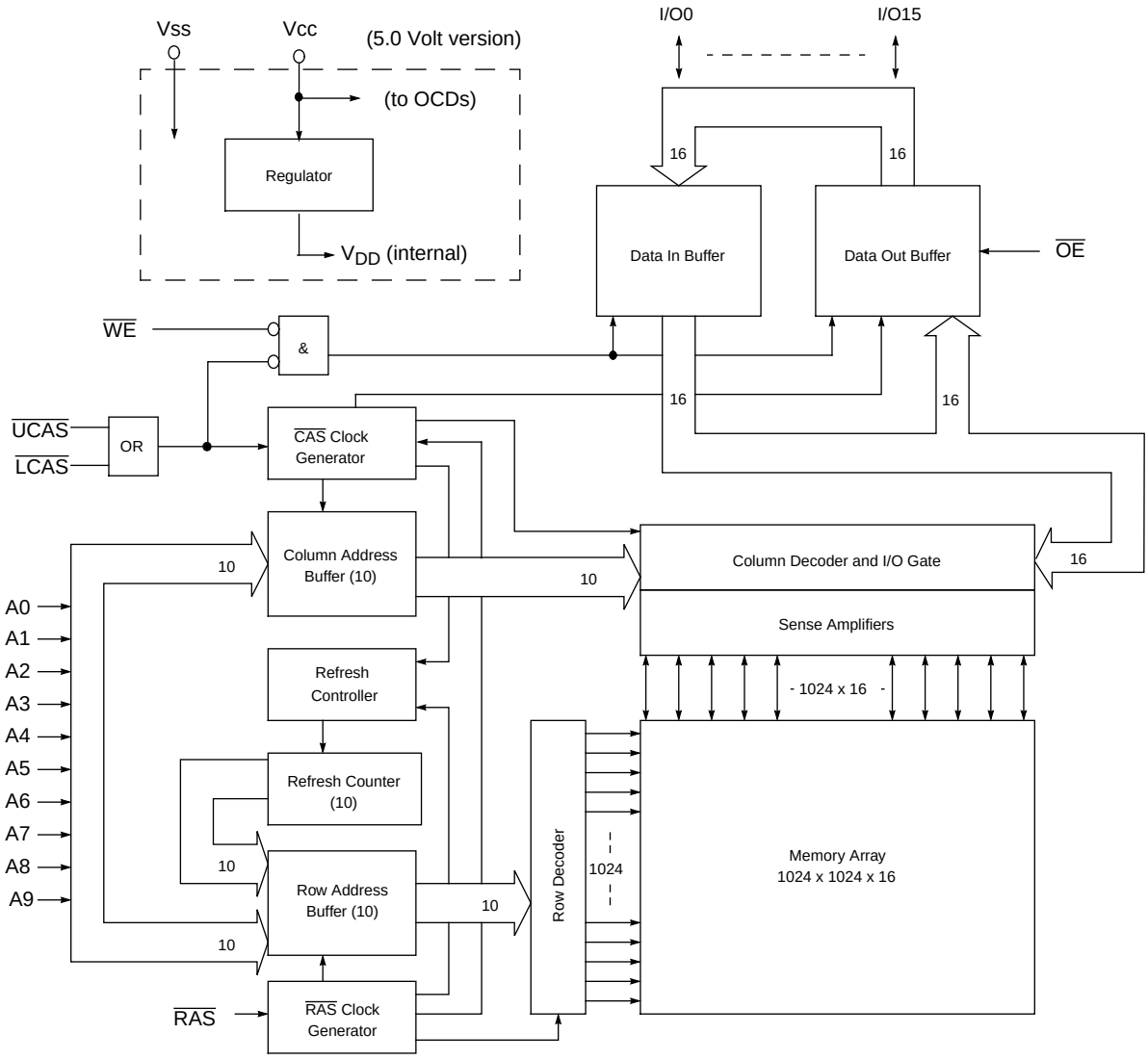
Ordering Information

Part Number	SP / LP	Self Refresh	Power Supply	Speed	Package	Notes
IBM0118160T3 -50	SP	No	5.0V	50ns	400mil TSOP-II 50/44	1
IBM0118160T3 -60	SP	No	5.0V	60ns	400mil TSOP-II 50/44	1
IBM0118160BT3 -50	SP	No	3.3V	50ns	400mil TSOP-II 50/44	1
IBM0118160BT3 -60	SP	No	3.3V	60ns	400mil TSOP-II 50/44	1
IBM0118160J3 -50	SP	No	5.0V	50ns	400mil SOJ 42/42	1
IBM0118160J3 -60	SP	No	5.0V	60ns	400mil SOJ 42/42	1
IBM0118160BJ3 -50	SP	No	3.3V	50ns	400mil SOJ 42/42	1
IBM0118160BJ3 -60	SP	No	3.3V	60ns	400mil SOJ 42/42	1
IBM0118160MT3 -50	LP	Yes	5.0V	50ns	400mil TSOP-II 50/44	1
IBM0118160MT3 -60	LP	Yes	5.0V	60ns	400mil TSOP-II 50/44	1
IBM0118160PT3 -50	LP	Yes	3.3V	50ns	400mil TSOP-II 50/44	1
IBM0118160PT3 -60	LP	Yes	3.3V	60ns	400mil TSOP-II 50/44	1
IBM0118160MJ3 -50	LP	Yes	5.0V	50ns	400mil SOJ 42/42	1
IBM0118160MJ3 -60	LP	Yes	5.0V	60ns	400mil SOJ 42/42	1
IBM0118160PJ3 -50	LP	Yes	3.3V	50ns	400mil SOJ 42/42	1
IBM0118160PJ3 -60	LP	Yes	3.3V	60ns	400mil SOJ 42/42	1

1. SP = Standard Power version (IBM0118160 and IBM0118160B); LP = Low Power version (IBM0118160M and IBM00118160P)

Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	I/O0 - I/O15
Standby		H	H→X	H→X	X	X	X	X	High Impedance
Read: Word		L	L	L	H	L	Row	Col	Data Out
Read: Lower Byte		L	L	H	H	L	Row	Col	Lower Byte: Data Out Upper Byte: High-Z
Read: Upper Byte		L	H	L	H	L	Row	Col	Lower Byte: High-Z Upper Byte: Data Out
Write: Word Early-Write		L	L	L	L	X	Row	Col	Data In
Write: Lower Byte Early-Write		L	L	H	L	X	Row	Col	Lower Byte: Data In Upper Byte: High-Z
Write: Upper Byte Early-Write		L	H	L	L	X	Row	Col	Lower Byte: High-Z Upper Byte: Data In
Read-Modify-Write		L	L	L	H→L	L→H	Row	Col	Data Out, Data In
Fast Page Mode Read	1st Cycle	L	H→L	H→L	H	L	Row	Col	Data Out
	2nd Cycle	L	H→L	H→L	H	L	N/A	Col	Data Out
Fast Page Mode Write	1st Cycle	L	H→L	H→L	L	X	Row	Col	Data In
	2nd Cycle	L	H→L	H→L	L	X	N/A	Col	Data In
Fast Page Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	H→L	L→H	Row	Col	Data Out, Data In
	2nd Cycle	L	H→L	H→L	H→L	L→H	N/A	Col	Data Out, Data In
$\overline{RAS}$-Only Refresh		L	H	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	L	H	X	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	L	H	L	Row	Col	Data Out
	Write	L→H→L	L	L	L→H	X	Row	Col	Data In
Self Refresh (LP version only)		H→L	L	L	H	X	X	X	High Impedance

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt Device	5.0 Volt Device		
V_{CC}	Power Supply Voltage	-0.5 to +4.6	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	-0.5 to min (V_{CC}+0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	-0.5 to min (V_{CC}+0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	1.0	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A= 0 to 70˚C)

Symbol	Parameter	3.3 Volt Device			5.0 Volt Device			Units	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of ≤ 4.0ns with 3.3 Volt, or V_{CC} + 2.0V for pulse widths of ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns) with 5.0 Volt. Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns with 3.3 Volt, or to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns) with 5.0 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A= 25°C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter	Min.	Max.	Units	Notes
C_{I1}	Input Capacitance (A0 - A9)	—	5	pF	1
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	—	7	pF	1
C_O	Output Capacitance (I/O0 - I/O15)	—	7	pF	1

1. Input capacitance measurements made with rise time shift method with $\overline{CAS}$ = V_{IH} to disable output.

DC Electrical Characteristics (T_A= 0 to +70˚C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter		Min.	Max.	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min.)	-50	—	120	mA	1, 2, 3
		-60	—	100		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		—	1	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	-50	—	120	mA	1, 3
		-60	—	100		
I_{CC4}	Fast Page Mode Current Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-50	—	30	mA	1, 2, 3
		-60	—	30		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)	SP version	—	1	mA	
		LP version	—	0.1		
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-50	—	120	mA	1, 3
		-60	—	100		
I_{CC7}	Self Refresh Current, LP version only Average Power Supply Current during Self Refresh CBR cycle with $\overline{RAS}$ ≥ t_{RASS} (min); $\overline{CAS}$ held low; $\overline{WE}$ = V_{CC} - 0.2V; Addresses and D_{IN} = V_{CC} - 0.2V or 0.2V.	3.3V	—	200	µA	
		5.0V	—	300		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3V)), All Other Pins Not Under Test = 0V		-5	+5	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-5	+5	µA	
V_{OH}	Output Level (TTL) Output “H” Level Voltage (I_{OUT} = -2.0mA for 3.3V, or I_{OUT} = -5mA for 5.0V)		2.4	V_{CC}	V	
V_{OL}	Output Level (TTL) Output “L” Level Voltage (I_{OUT} = +2.0mA for 3.3V, or I_{OUT} = +4.2mA for 5.0V)		0.0	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ =V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ =V_{IH}.

AC Characteristics (T_A= 0 to +70˚C, V_{CC}= 3.3V 0.3V or V_{CC}= 5.0V 0.5V)

1. In initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16 bits of data are read/written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ cannot be staggered within the same read/write cycle.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	95	—	110	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	—	40	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	60	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	13	10K	15	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	37	20	45	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	25	15	30	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	13	—	15	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	50	—	60	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	ns	3
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	3
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	4

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Either t_{DZC} or t_{DZO} must be satisfied.
4. AC measurements assume t_T=5ns.

Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	13	—	15	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	13	—	15	—	ns	
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	13	—	15	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	3
t_{DH}	D_{IN} Hold Time	10	—	12	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
2. Either t_{CDD} or t_{OED} must be satisfied.
3. These parameters are referenced to $\overline{LCAS}$ or $\overline{UCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.

Read Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{CAS}$	—	13	—	15	ns	1, 3
t_{AA}	Access Time from Address	—	25	—	30	ns	2, 3
t_{OEA}	Access Time from $\overline{OE}$	—	13	—	15	ns	3
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	4
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	25	—	30	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	3
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{OHO}	Output Data Hold from $\overline{OE}$	3	—	3	—	ns	
t_{OFF}	Output Buffer Turn-Off Delay	—	13	—	15	ns	5
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	—	13	—	15	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	—	15	—	ns	6

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current load and 100pF.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{CDD} or t_{OED} must be satisfied.

Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	128	—	150	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	68	—	80	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	31	—	35	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	43	—	50	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	13	—	15	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

Fast Page Mode Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{PC}	Fast Page Mode Cycle Time	35	—	40	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	50	200K	60	200K	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	28	—	35	ns	1
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	—	35	—	ns	

1. Measured with the specified current load and 100pF.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	71	—	80	—	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	48	—	55	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	

Self Refresh Cycle - Low Power Version Only

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RASS}	$\overline{RAS}$ Pulse Width During Self Refresh Cycle	100	—	100	—	µs	1
t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	89	—	104	—	ns	1
t_{CHS}	$\overline{CAS}$ Hold Time From RAS Rising During Self Refresh Cycle	-50	—	-50	—	ns	1, 2
t_{CHD}	$\overline{CAS}$ Hold Time From RAS Falling During Self Refresh Cycle	350	—	350	—	µs	1, 2

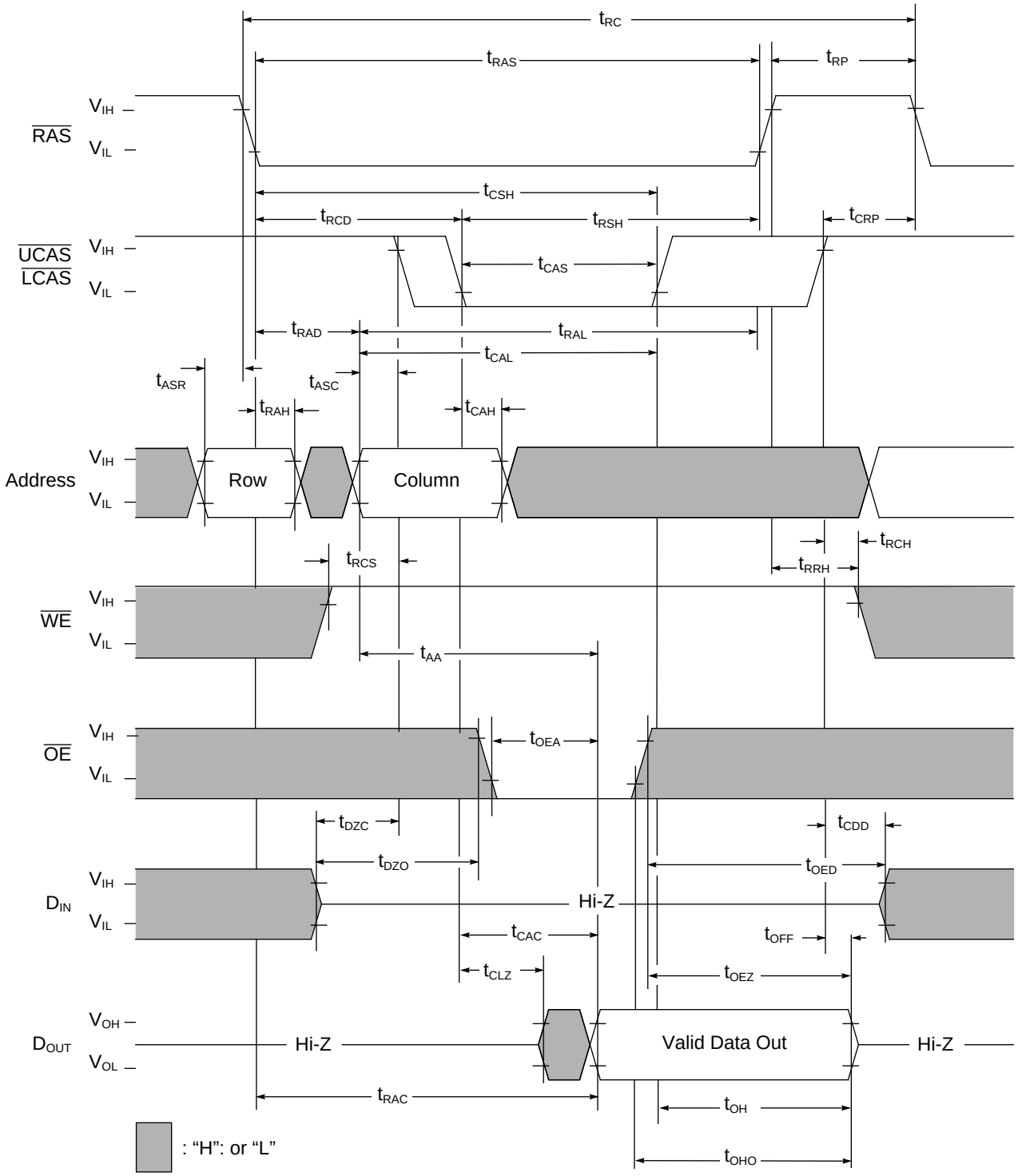
1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
   If row addresses are being refreshed in an EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.
   If row addresses are being refreshed in any other manner (ROR- Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.
2. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies. If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

Refresh

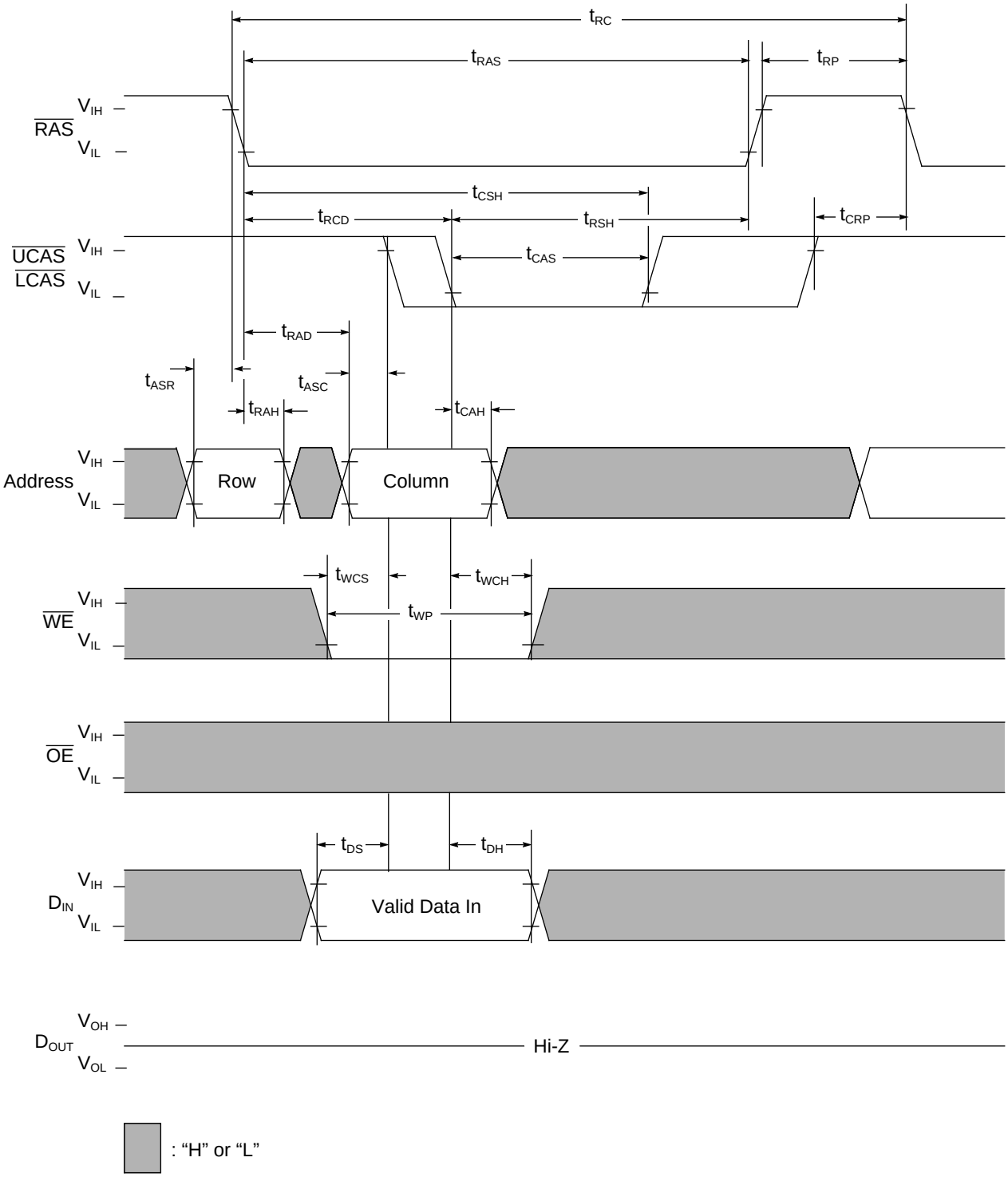
Symbol	Parameter		-50		-60		Units	Notes
			Min.	Max.	Min.	Max.		
t_{REF}	Refresh Period	SP version	—	16	—	16	ms	1
		LP version	—	128	—	128		

1. 1024 cycles.

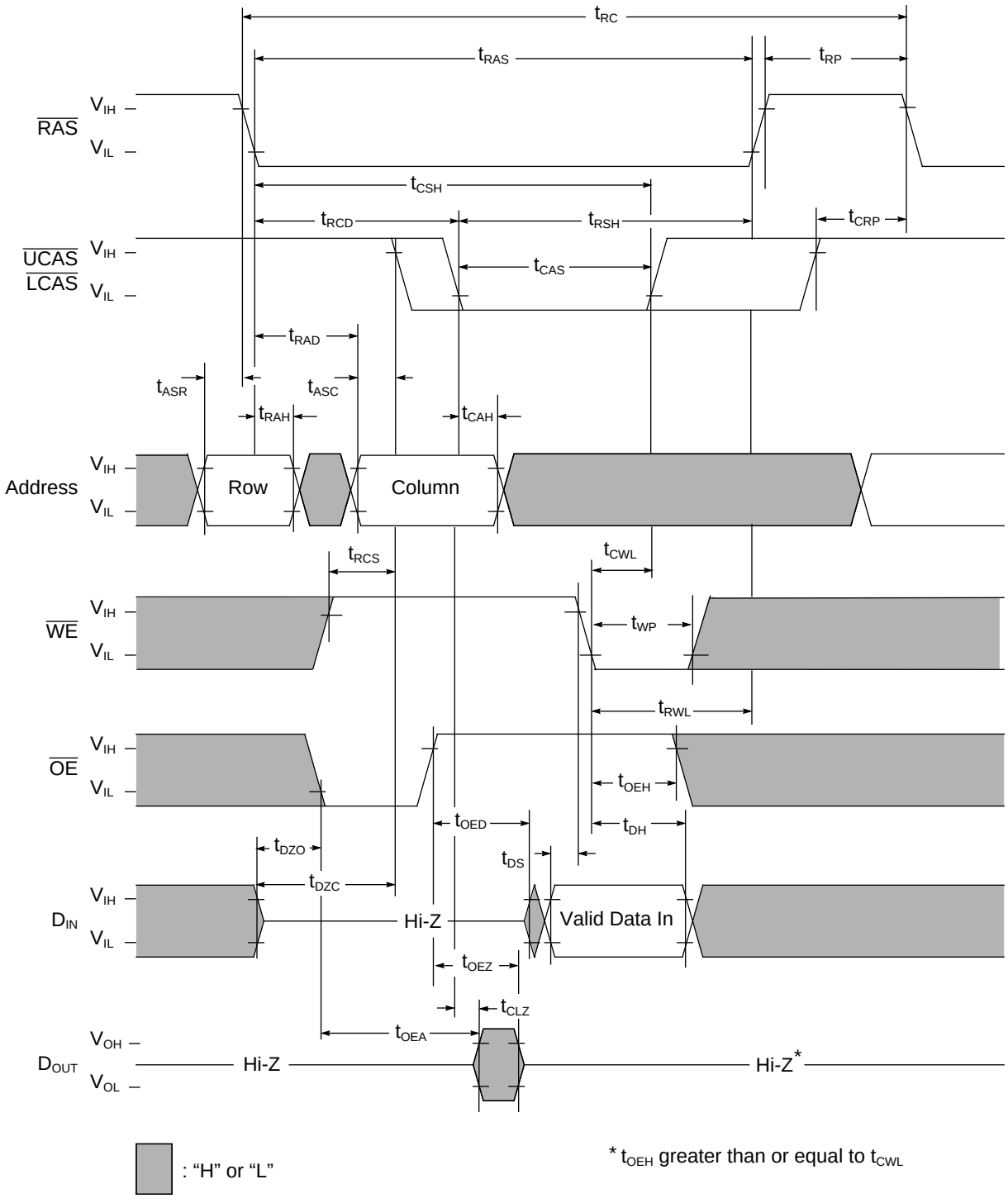
Read Cycle



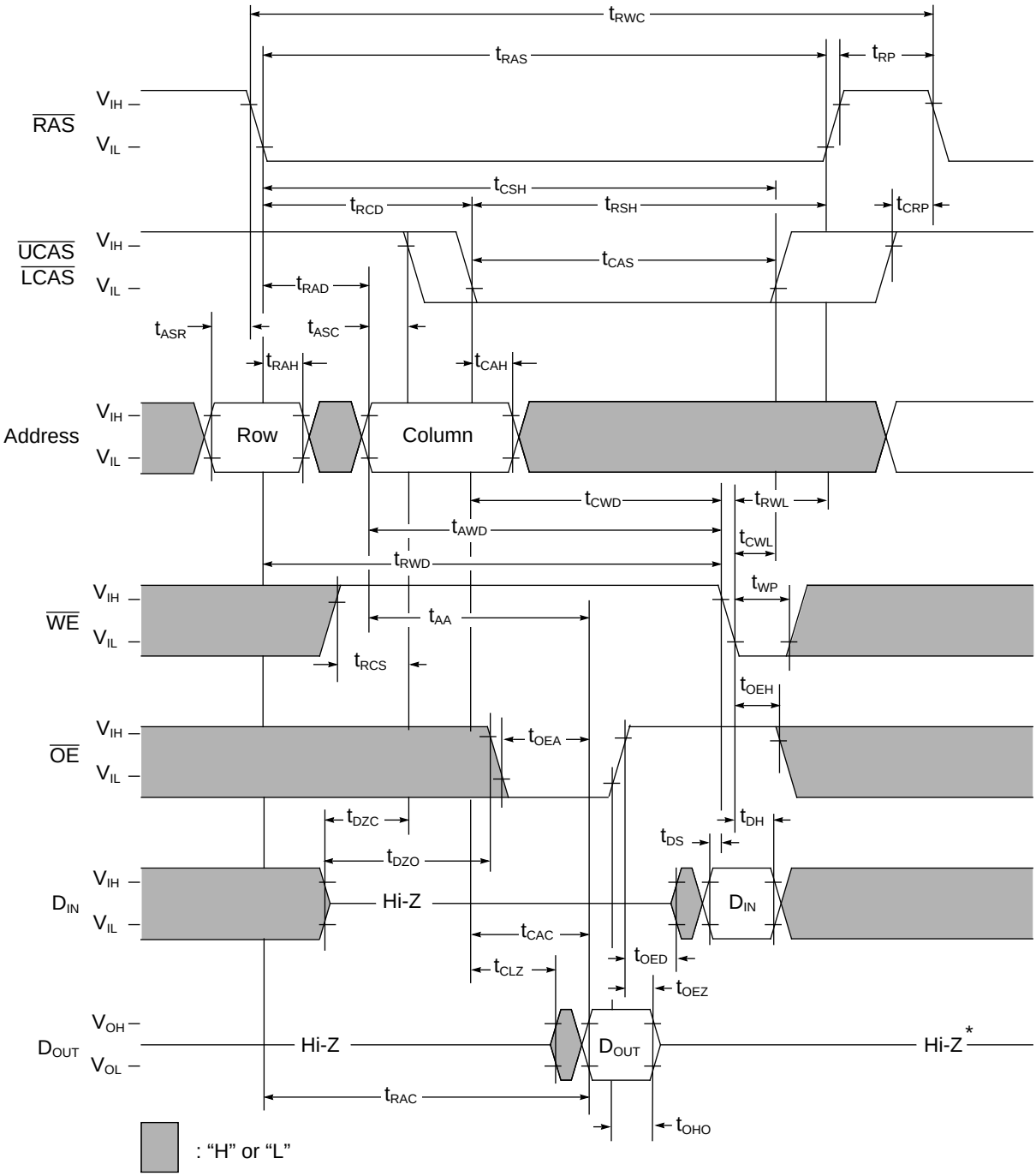
Write Cycle (Early Write)



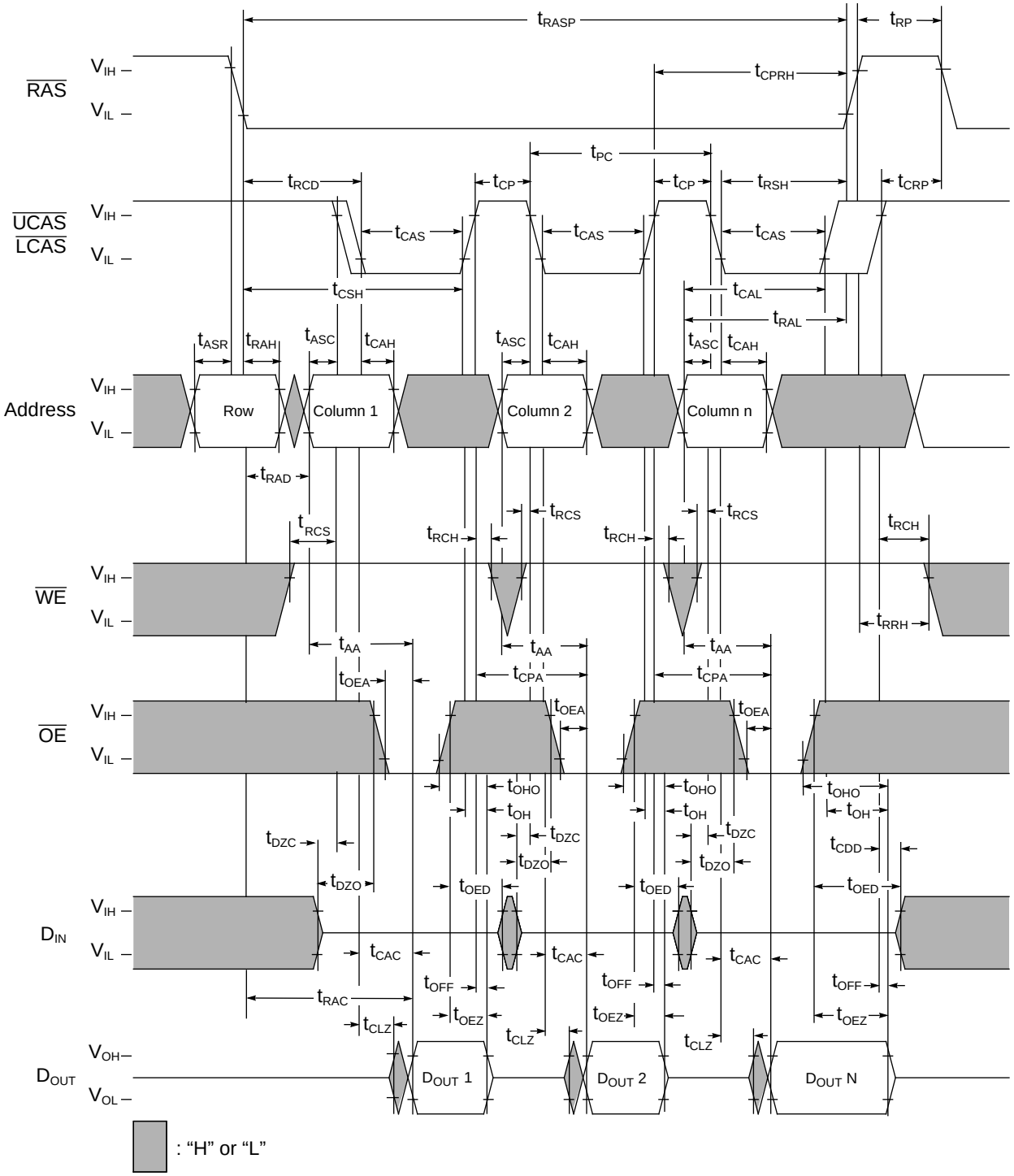
Write Cycle (Delayed Write)



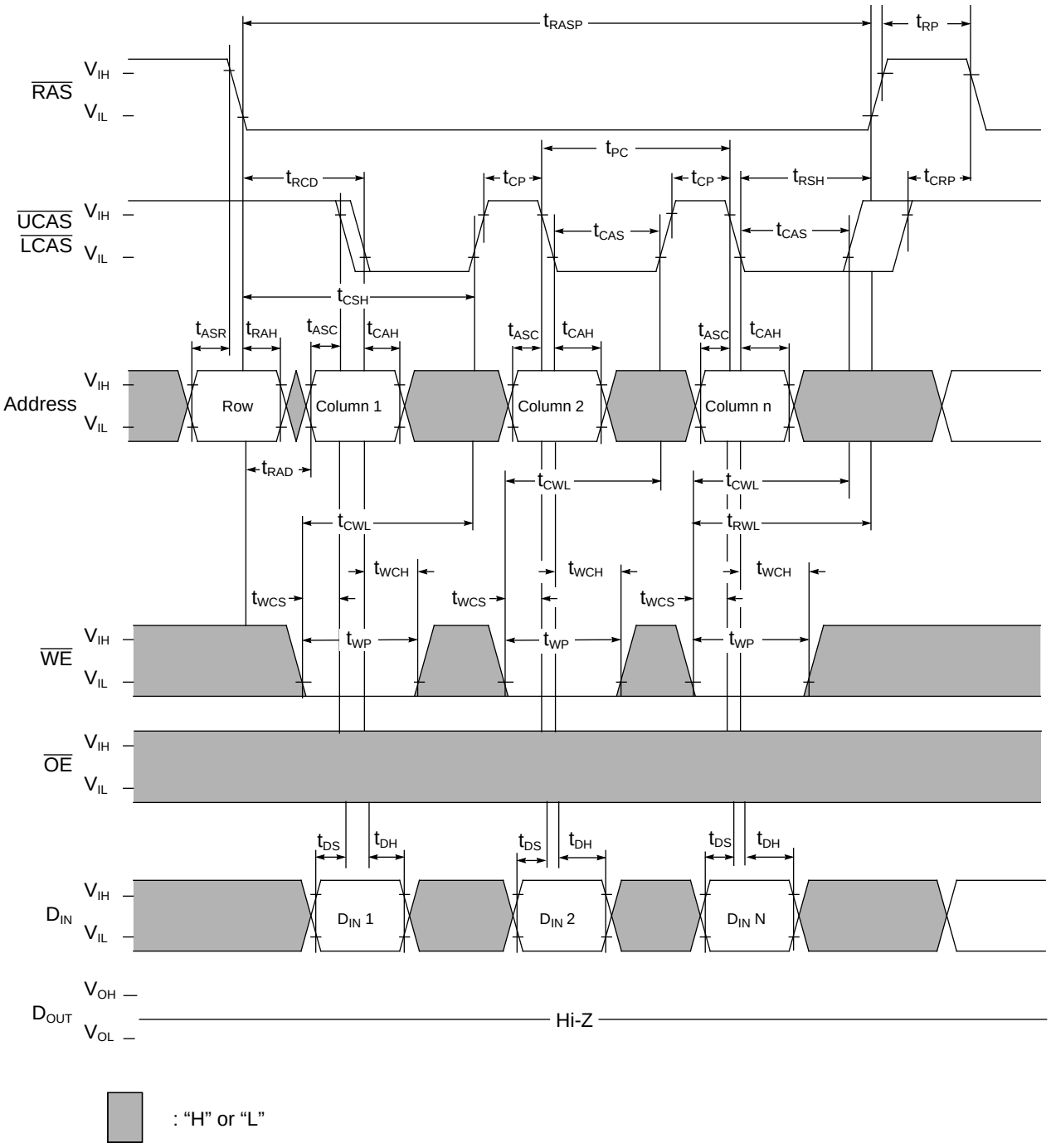
Read-Modify-Write Cycle



Fast Page Mode Read Cycle

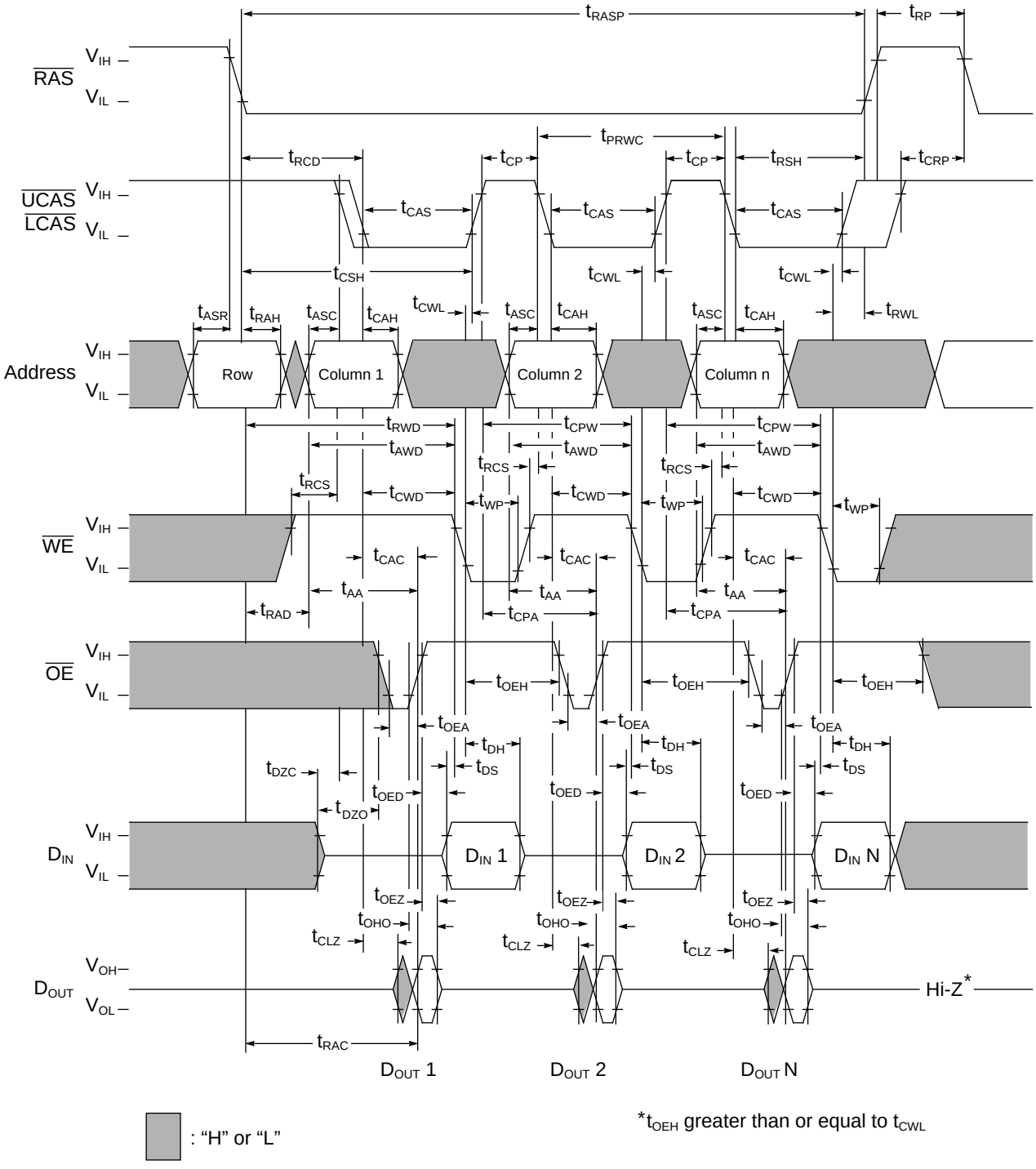


Fast Page Mode Write Cycle

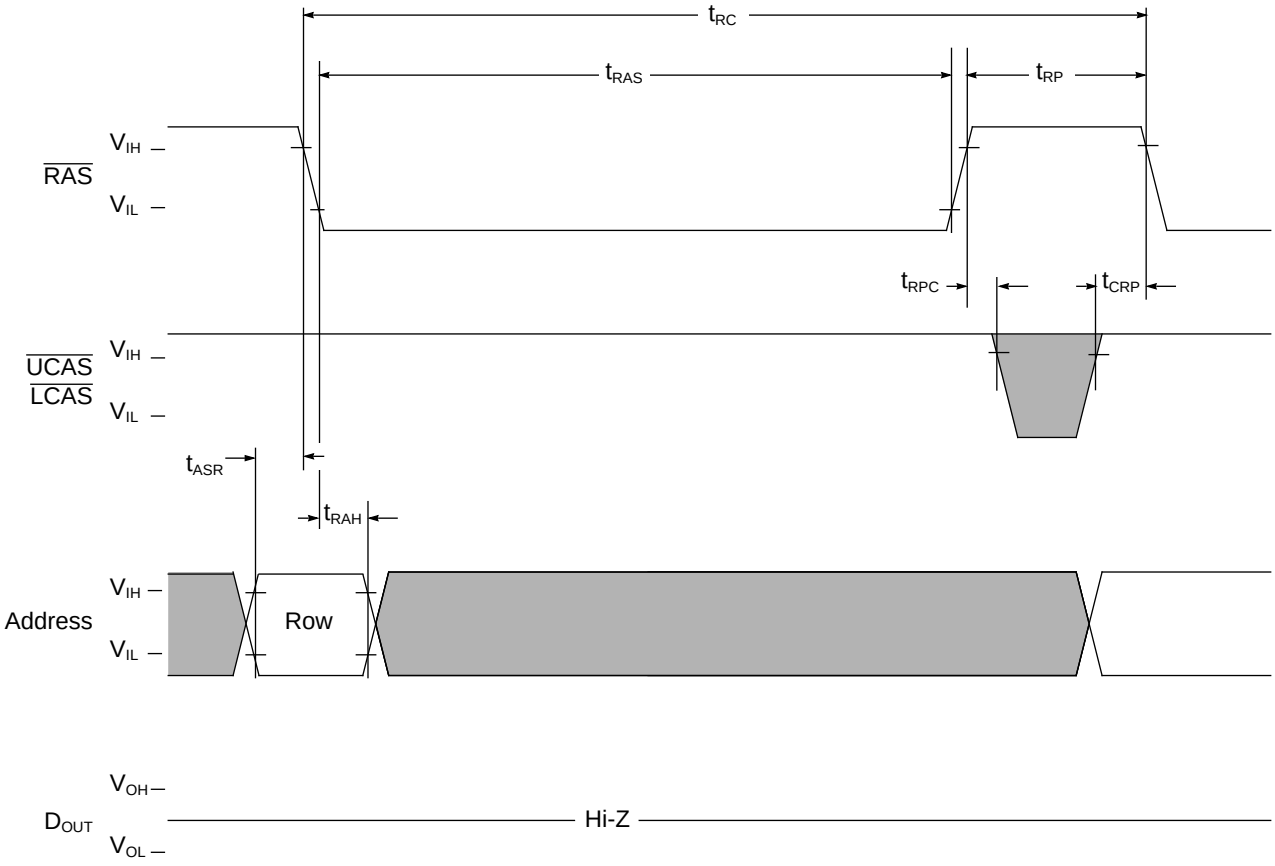


: “H” or “L”

Fast Page Mode Read-Modify-Write Cycle



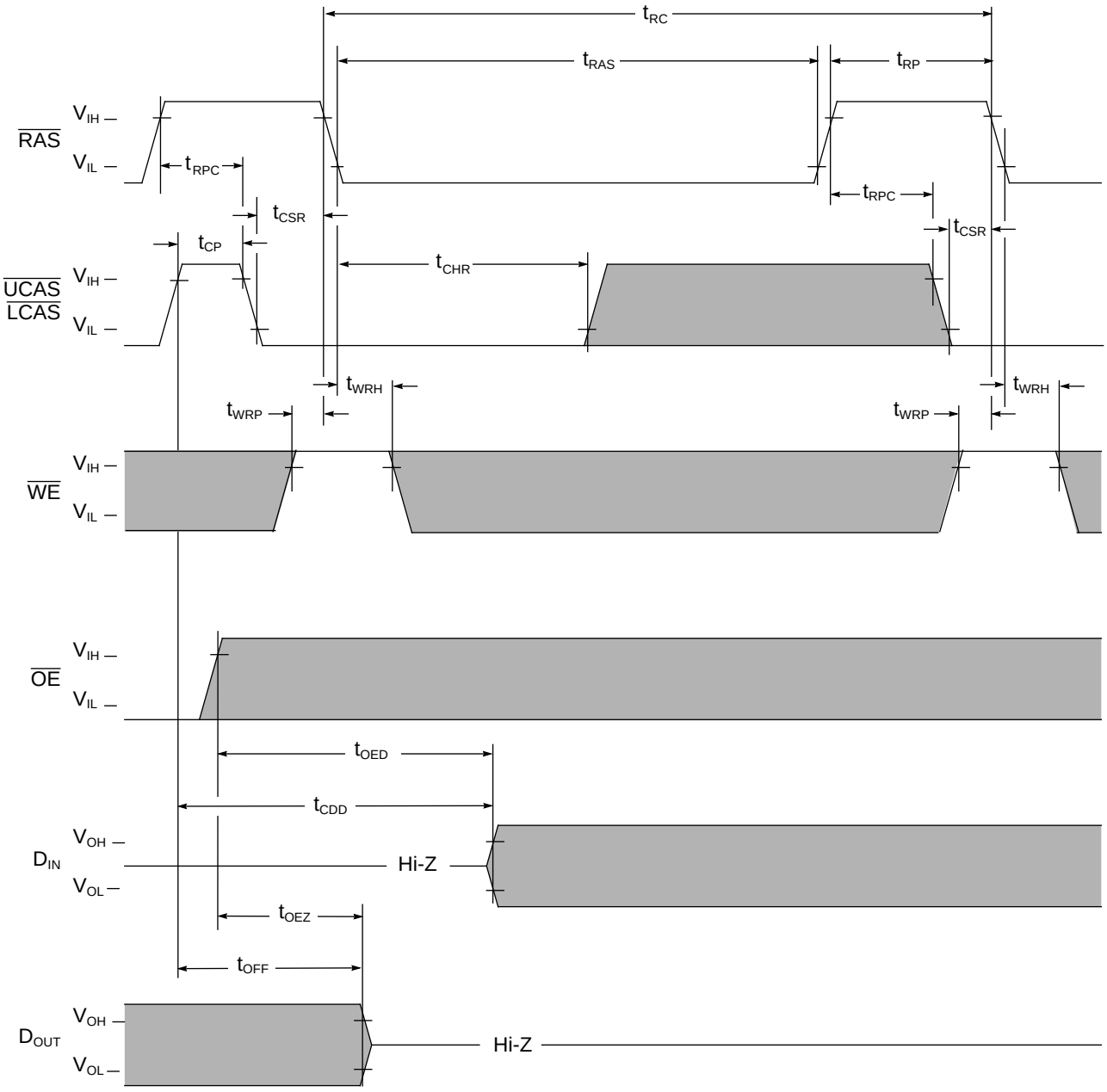
$\overline{RAS}$ Only Refresh Cycle



: “H” or “L”

NOTE: $\overline{WE}$, $\overline{OE}$ and D_{IN} are “H” or “L”

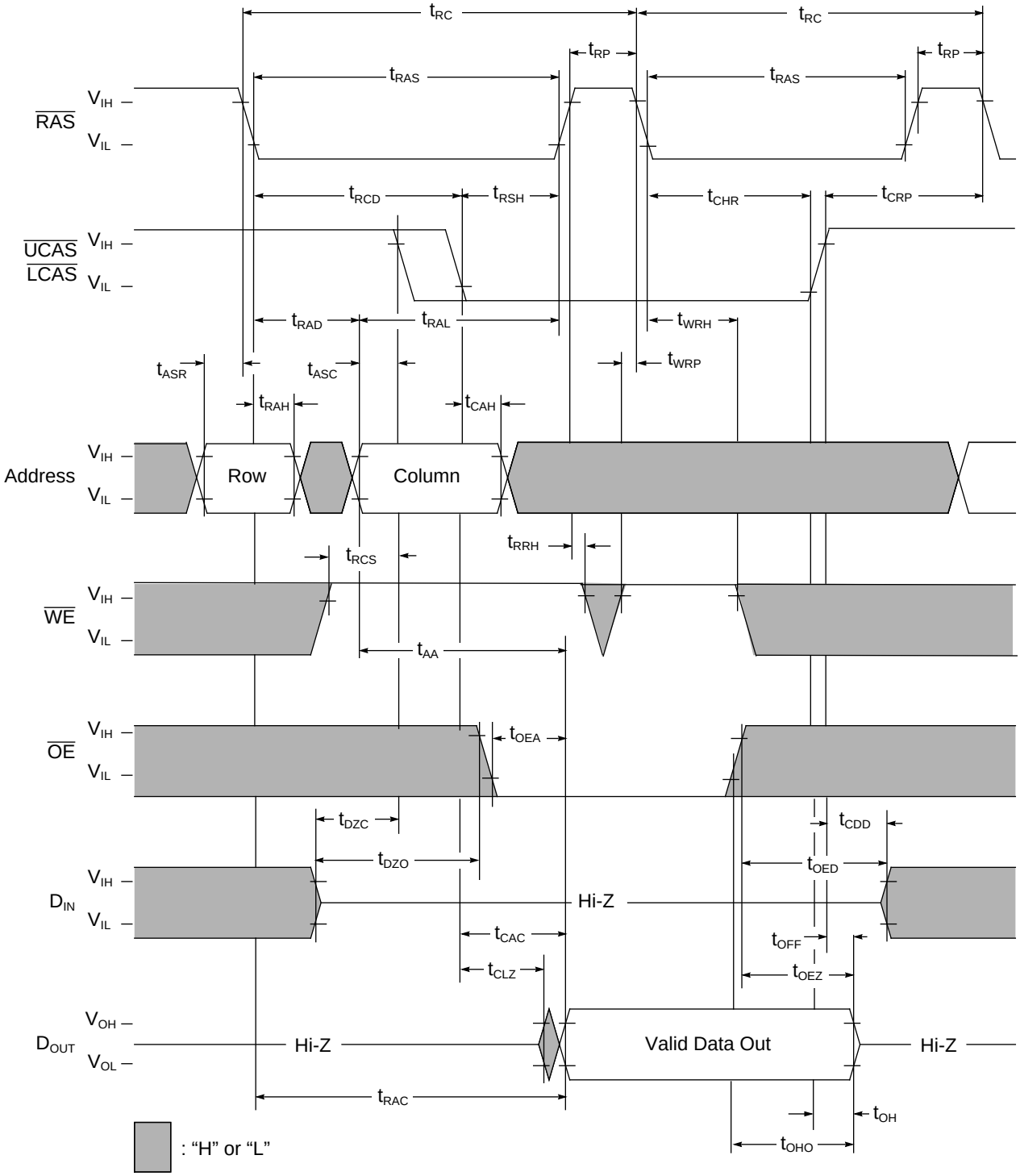
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



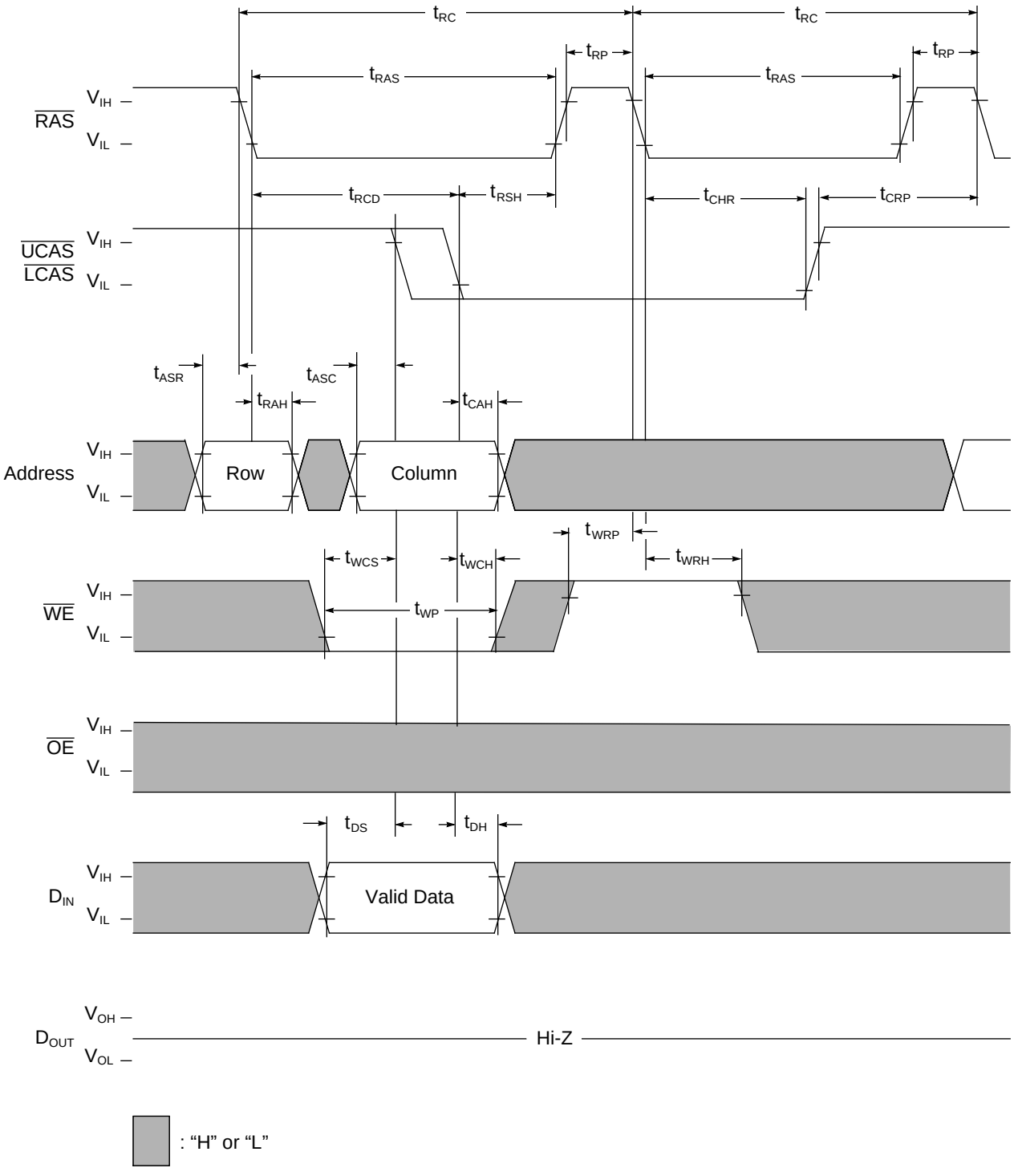
: "H" or "L"

NOTE: Address is "H" or "L"

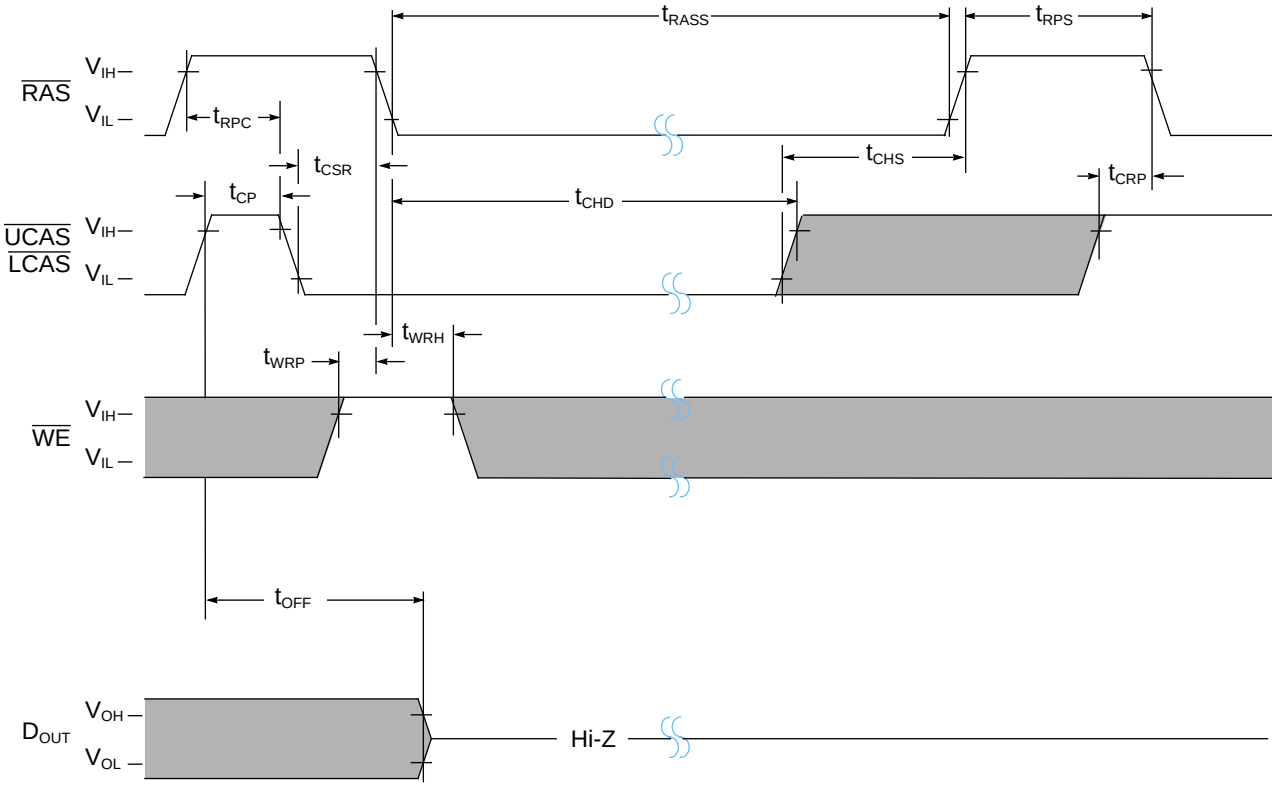
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Self Refresh Cycle (Sleep Mode) - Low Power version only

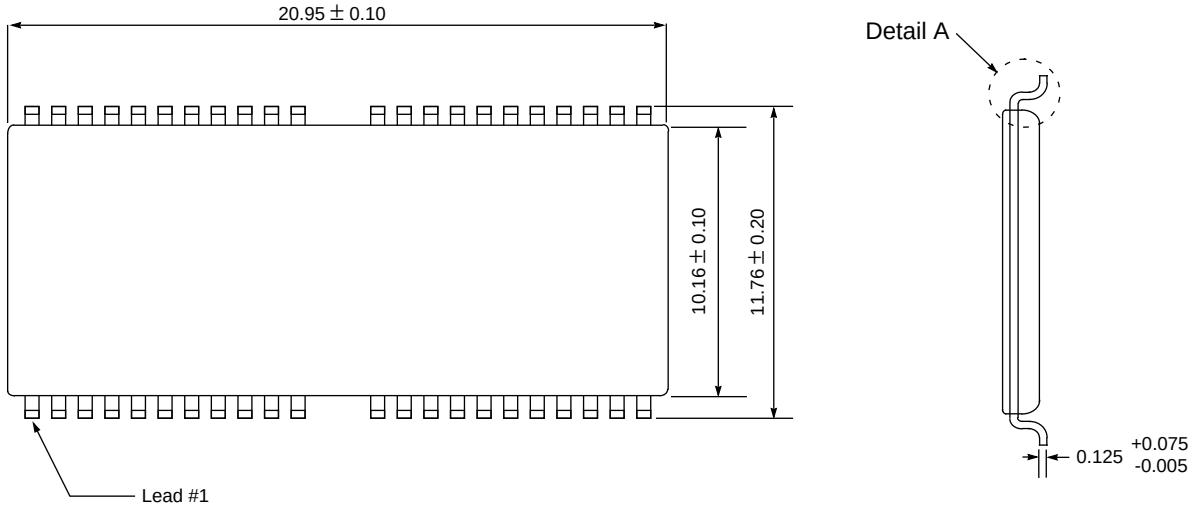


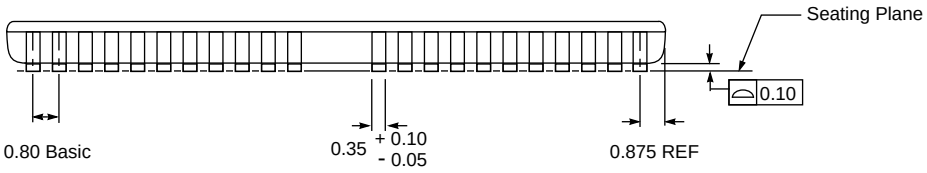
: "H" or "L"

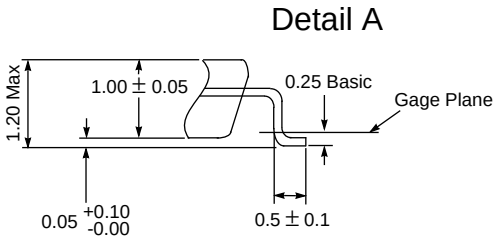
NOTES:

1. Address and $\overline{OE}$ are "H" or "L"
2. Once $\overline{RAS}$ (min) is provided and $\overline{RAS}$ remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."
3. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies.
   If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

PACKAGE DIMENSIONS (400mil; 50/44 lead; Thin Small Outline Package)

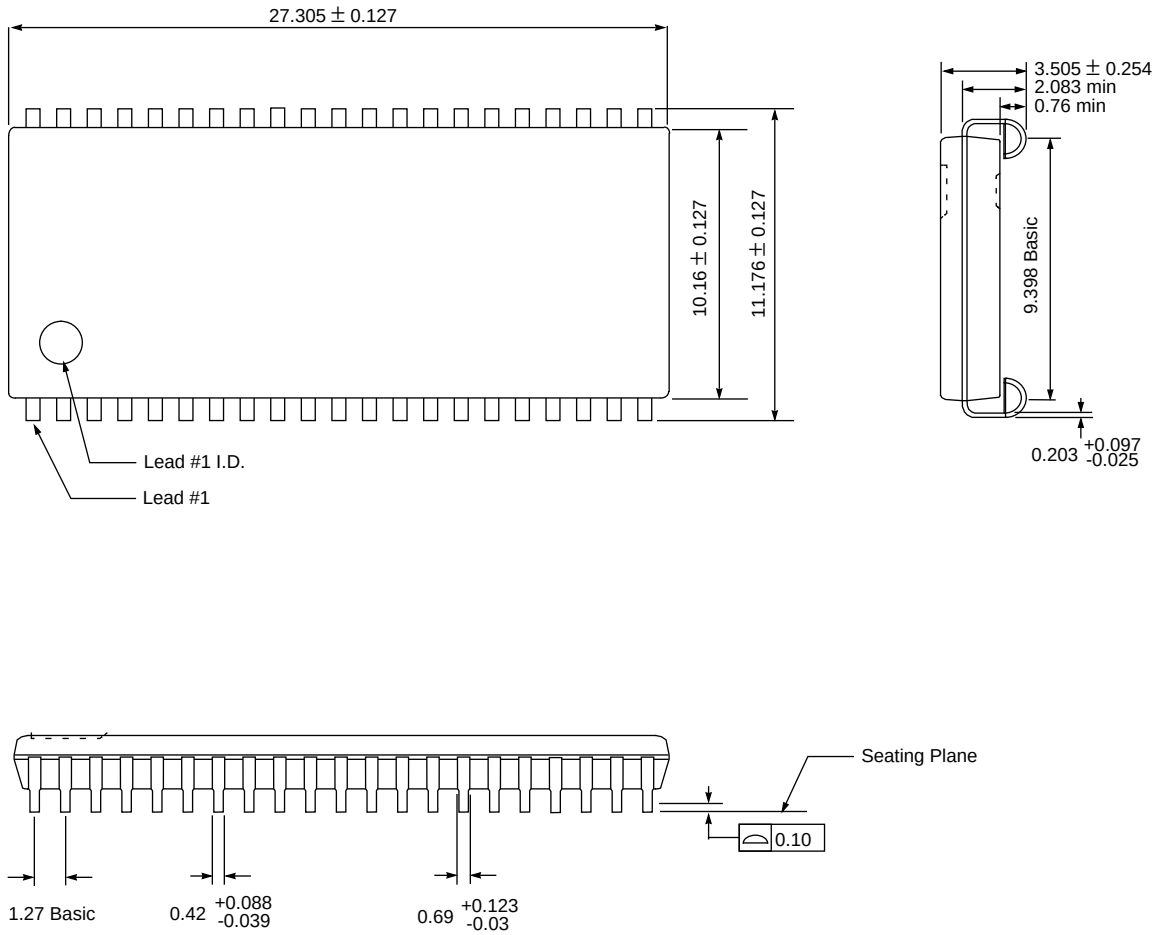






NOTE: All dimensions are in millimeters; Package diagrams are not drawn to scale.

PACKAGE DIMENSIONS (400mil; 42/42 lead; Small Outline J-Lead)



NOTE: All dimensions are in millimeters; Package diagrams are not drawn to scale.

Revision Log

Revision	Contents Of Modification
01/94	Initial Release
06/17/94	Change Fast Page Mode Currents (I_{CC4}) from 85, 75, 65, 55mA to 100, 90, 80, 70mA
09/06/94	Combine the 3.3 Volt and the 5.0 Volt specifications Change the Refresh Period from 256ms to 128ms Change I_{CC1}, I_{CC3}, I_{CC6} from 215, 195, 170, 150mA to 225, 205, 180, 160mA
11/15/95	1. Iout changed to +2.0 mA and -2.0 mA in DC Electrical Characteristics table. 2. Packaging diagrams modified to clarify lead thickness and standoff height. 3. t_{RPC} min changed from 0 to 5ns. 4. t_{CHR} min changed from 20 to 10ns. 5. Currents in DC Electrical Characteristics table revised. 6. Test Modes and Test Circuit Diagram removed. 7. Rename t_{ODD} to t_{OED}. 8. t_{OED}, t_{CDD}, t_{OEZ}, and t_{OFF} min changed from 20 to 15ns, for the 70ns part. 9. t_{RRH} min changed from 5 to 0ns for all speed sorts. 10. t_{OEH} min changed from 20 to 15ns for the 70ns part. 11. t_{CSR} min changed from 5 to 10ns for all speed sorts. 12. tCAH min changed from 15 to 10ns on 60 and 70ns parts. 13. t_{OFF} max changed from 20 to 15ns for 70ns parts.
12/10/95	1. The Low Power and Standard Power Specifications were combined. ES# 43G9387 and ES# 43G9388 were combined into ES# 43G9388. 2. Added Die Rev E part numbers. 3. t_{DH} was reduced from 15ns to 12ns for the -60 speed sort. 4. t_{CHD} was added to the Self Refresh Cycle with a value of 350µs for all speed sorts. 5. The Self Refresh timing diagram was changed to allow $\overline{CAS}$ to go high t_{CHD} (350µs) after $\overline{RAS}$ falls entering a Self Refresh. 6. The CBR timing diagram was changed to allow $\overline{CAS}$ to remain low for back-to-back CBR cycles. 7. $\overline{WE}$ for the Hidden Refresh Write cycle in the Truth Table was changed from “L” to ” H”.
09/01/96	1. I_{CC2} was changed from 2mA to 1mA. 2. $I_{I(L)}$ and $I_{O(L)}$ were altered from +/- 10uA to +/- 5uA. 3. t_T was initially at a max of 30ns. It has been modified to 50ns for all speed sorts. 4. t_{CPA} was decreased from 30ns to 28ns for the -50 speed sort. 5. t_{RASP} max of 125K was raised to 200K for all speed sorts. 6. t_{RP} was changed from 35ns to 30ns for the -50 speed sort.

Revision Log

03/19/97	1. $\overline{WE}$ for the Hidden Refresh Write cycle in the Truth Table was changed from “H” to “L→H”. 2. t_{OED} was moved from the Common Parameters table to the Write Cycle Parameters Table. 3. t_{ODD} in the $\overline{CAS}$ before $\overline{RAS}$ timing diagram was renamed t_{OED}. 4. The -70 speed sort and timings were removed. 5. I_{cc1}, I_{cc3}, I_{cc6} for the -50 speed sort were reduced from 185mA to 120mA. 6. I_{cc4} for the -50 speed sort was reduced from 100mA to 30mA. 7. I_{cc1}, I_{cc3}, I_{cc6} for the -60 speed sort were reduced from 160mA to 100mA. 8. I_{cc4} for the -60 speed sort was reduced from 90mA to 30mA.
04/23/97	1. I_{cc5} was changed from 200µA to 100µA for the Low Power Die Rev F Parts.

Discontinued (9/98 - last order; 3/99 last ship)

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